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Title:	Radiation Effects on Electronics: How to Destroy a Satellite in Three Easy Steps
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Radiation Effects on Electronics

How to Destroy a Satellite in Three Easy Steps

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6/4/2019

National Nuclear Security Administration
Managed by Triad National Security, LLC for the U.S. Department of Energy's NNSA

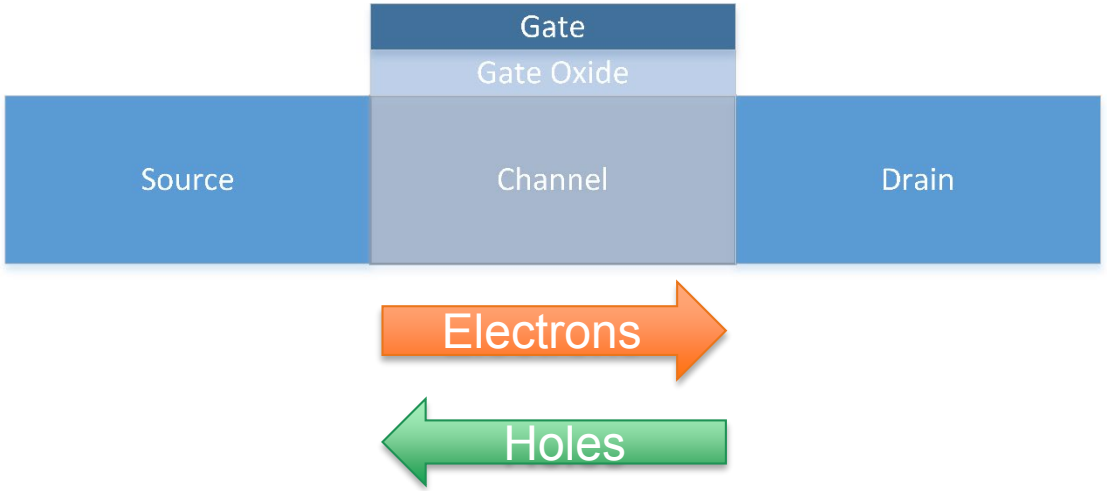
Radiation Effects Electronics

- **The world's quickest introduction to transistors**
- **Three dominant effects**
  - Total ionizing dose (TID)
  - Displacement damage (DD), or Total Non-Ionizing Dose (TNID)
  - Single-event effects (SEEs)

5 Minute Overview of Transistors

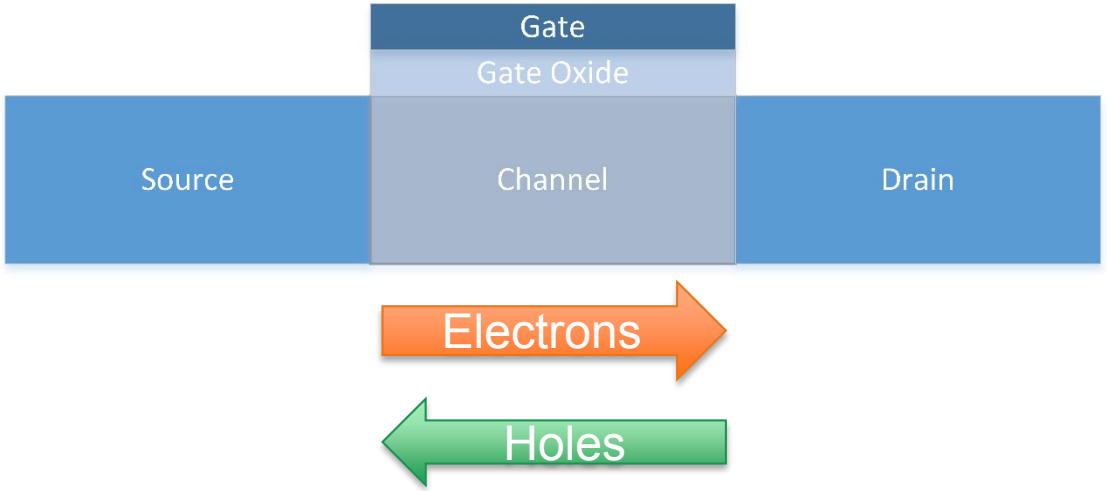
Transistor Structures

- **Transistors are the building block of digital electronics**
  - When the transistor is on, there is charge flow in the channel
- **The transistor properties depend on a very rigid lattice structure and design**
  - Electrons need to be where they are expected to be
  - Holes need to be where they are expected to be
- **As feature sizes have shrunk the amount of atoms in each area has drastically shrunk**
  - Harder to maintain the properties when there are so few atoms in the design
  - Harder to manufacture the structures



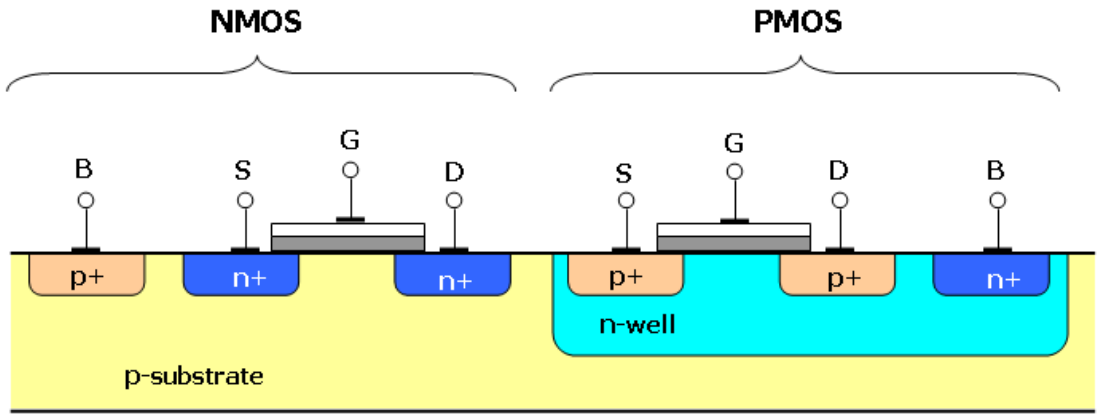
Transistor Materials

- **Modern transistors have p+ and p material the source and drain, n type materials in the channel**
- **The transistors are packed end to end**
  - Create another transistor with little space between transistors
- **Most commonly, the transistor is on top of a substrate (“the body”)**
  - Most common substrate it a p type
  - Sometimes the substrate will have a layer of n+ type and then a layer of p type
    - Creates a vertical transistor without a gate
- **Invariably, all of the extra transistors are uncontrolled and have radiation issues**



Transistor Wells

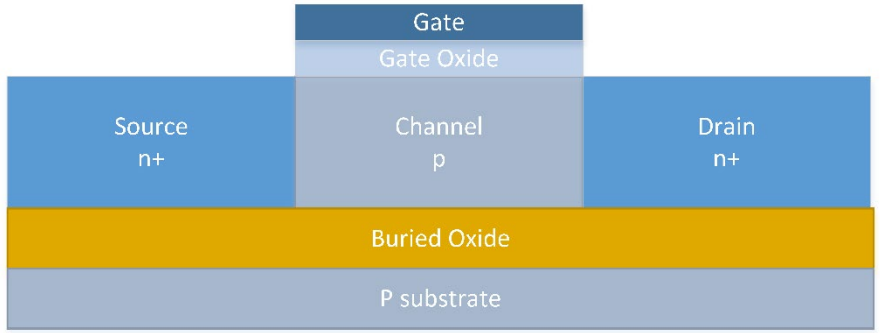
- **Many transistors will use material wells to isolate one type from another type**
  - The source and drain of the PMOS transistor creates two vertical transistors
  - There is a horizontal transistor between the NMOS and PMOS transistors
- **Notice that substrate running across the bottom**
  - If radiation create charge generation in the p substrate, it can spread to multiple transistors
  - With modern electronics, the size of the charge generation “cloud” or region from the radiation is >> a single transistor



By Reza Mirhosseini - originally uploaded to en.wikipedia (file log), Public Domain, https://commons.wikimedia.org/w/index.php?curid=12271062

Buried Oxide (B_{ox}) Transistors

- **The buried oxide**
  - Keeps charge from collecting under the channel
  - Isolates the channel from the substrate so that charge cannot go upward from the substrate to the channel
- **Many radiation-hardened electronics use Box transistors: Silicon on insulator (SOI)**
  - Often very good for some radiation effects and irrelevant for others
  - It also has to be designed correctly, and there are designers who have screwed it up



Total Ionizing Dose (TID)

Total Ionizing Dose (TID)

- **Historically, the dominant problem for satellites**
  - Caused by most forms of charged particles, but not neutrals
- **Prolonged exposure to ionizing radiation can cause "MOSFET threshold voltage shift, increased leakage current, and degraded timing parameters" [L. D. Edmonds, C. E. Barnes, and L. Z. Scheick, "An introduction to space radiation effects on microelectronics," Tech. Rep., 2000, Available at http://parts.jpl.nasa.gov/docs/JPL00-62.pdf]**
- **These parametric changes cause essentially an accelerated aging effect that leads to often permanent failure of the electronic component**
  - In some cases it is possible to anneal the effect, but generally annealing deployed electronics is not possible

TID Mechanisms

- **From [Barnaby2006], "The physical processes that lead from the initial deposition of energy by ionizing radiation to the creation of ionization defects are:**
  1. the generation of ehps [electron-hole pairs],
  2. the prompt recombination of a fraction of the generated ehps,
  3. the transport of free carriers remaining in the oxide, and
  4. either the formation of trapped charge via hole trapping in defect precursor sites or the formation of interface traps via reactions involving hydrogen"
- **In lay terms: the charge particle has transported the electrons and the holes into all of the wrong places**
  - Much of the radiation-hardened by process (RBHP) methodology is designing transistors that by nature do not have these issues (SOI, annular)

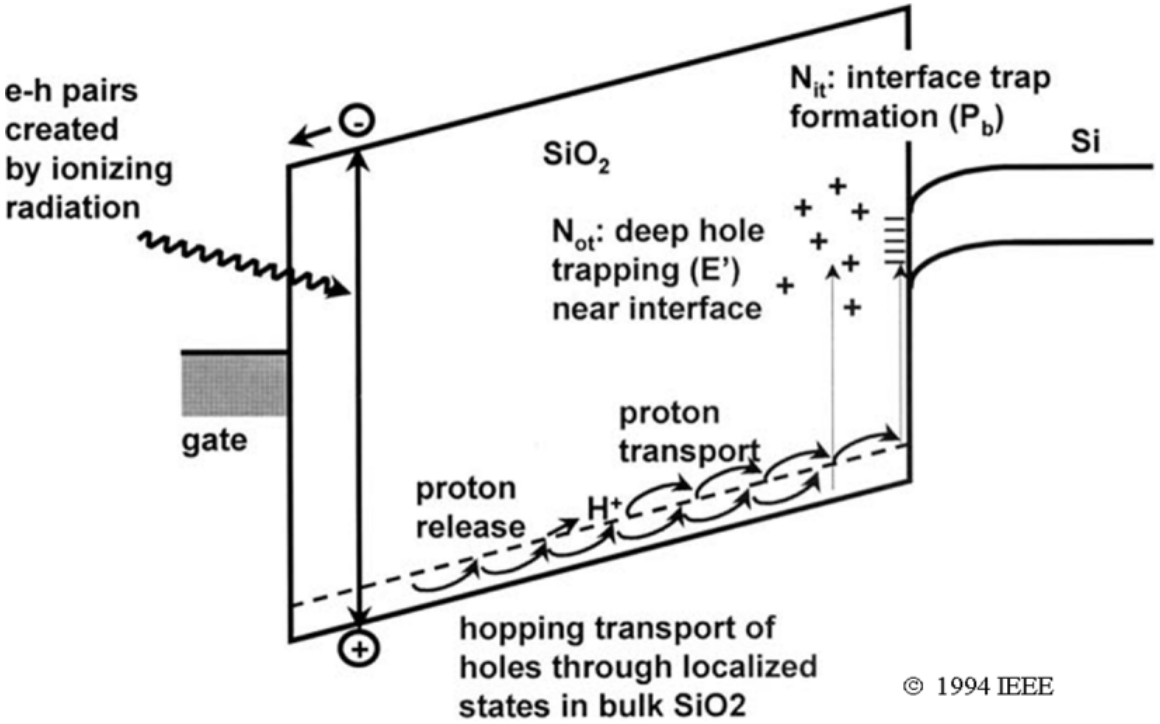


Illustration of the main processes in TID damage [H. J. Barnaby, "Total-Ionizing-Dose Effects in Modern CMOS Technologies," in *IEEE Transactions on Nuclear Science*, vol. 53, no. 6, pp. 3103-3121, Dec. 2006.]

Theoretical TID Effects on Electronics: Trapped Charge

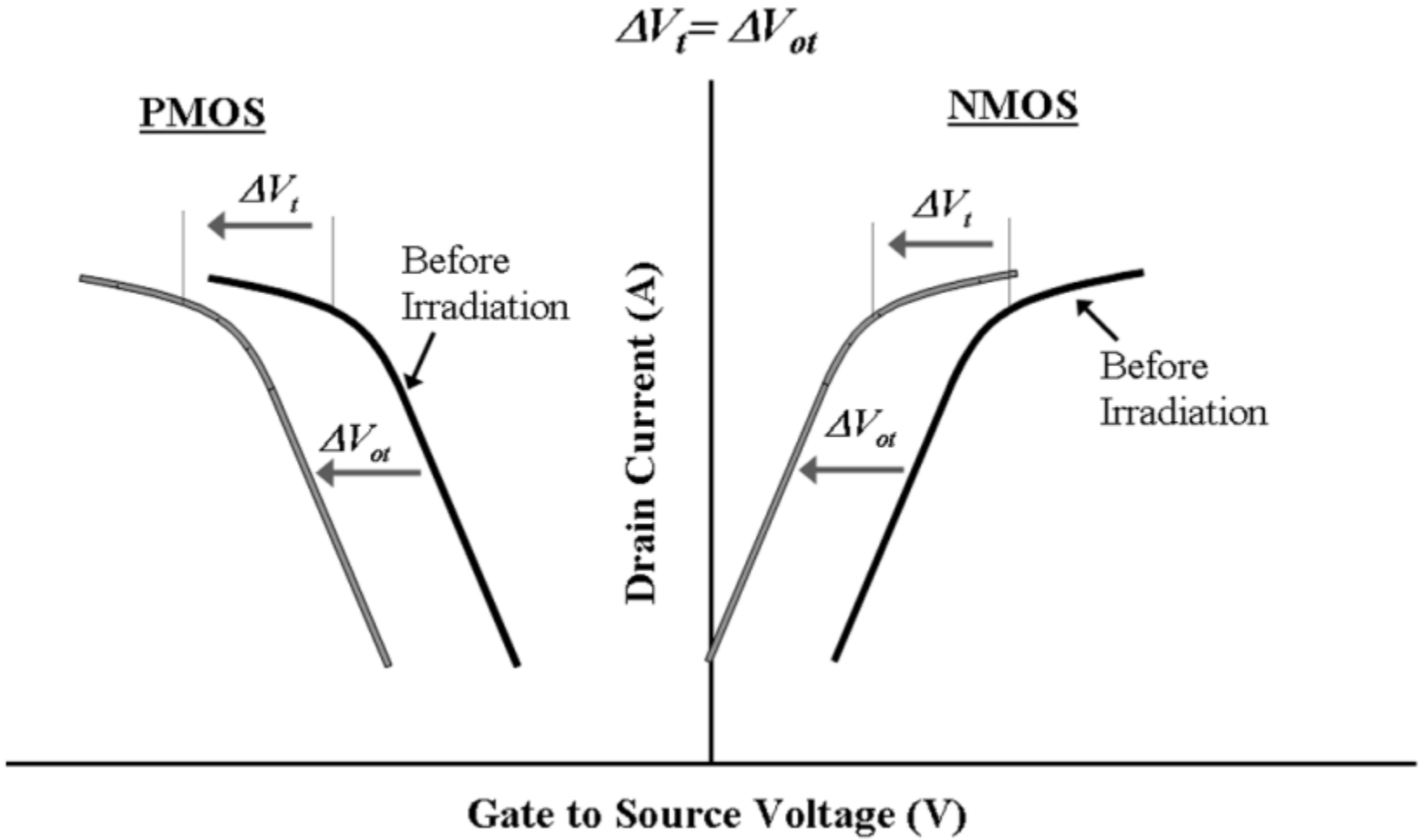


Illustration of the effect of fixed oxide trapped charge on n- and p-MOS devices.
[H. J. Barnaby, "Total-Ionizing-Dose Effects in Modern CMOS Technologies," in *IEEE Transactions on Nuclear Science*, vol. 53, no. 6, pp. 3103-3121, Dec. 2006.]

Theoretical TID Effects on Electronics: Interface Traps

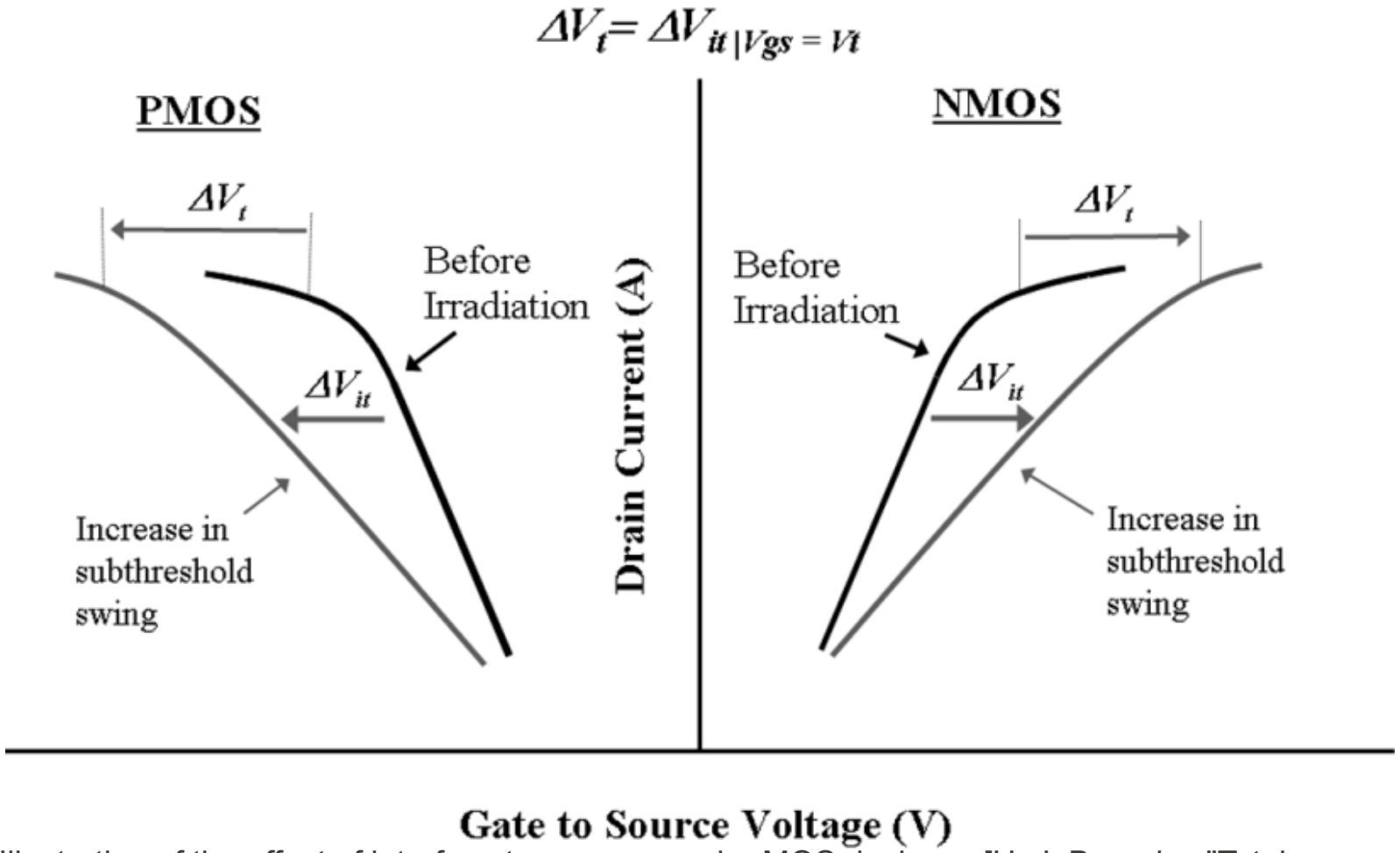
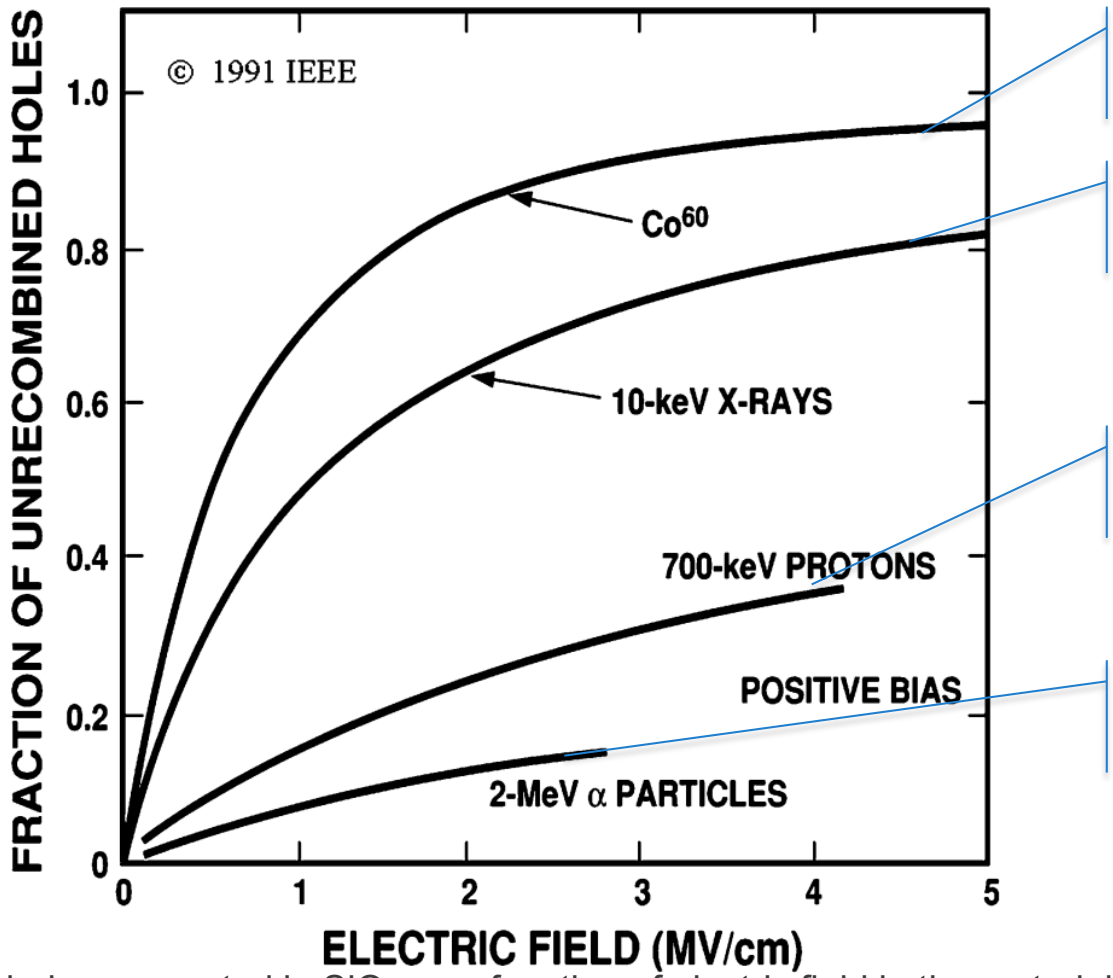


Illustration of the effect of interface traps on n- and p-MOS devices. [H. J. Barnaby, "Total-Ionizing-Dose Effects in Modern CMOS Technologies," in *IEEE Transactions on Nuclear Science*, vol. 53, no. 6, pp. 3103-3121, Dec. 2006.]

Types of Radiation and TID Efficiency



Gammacell

GPS

LEO

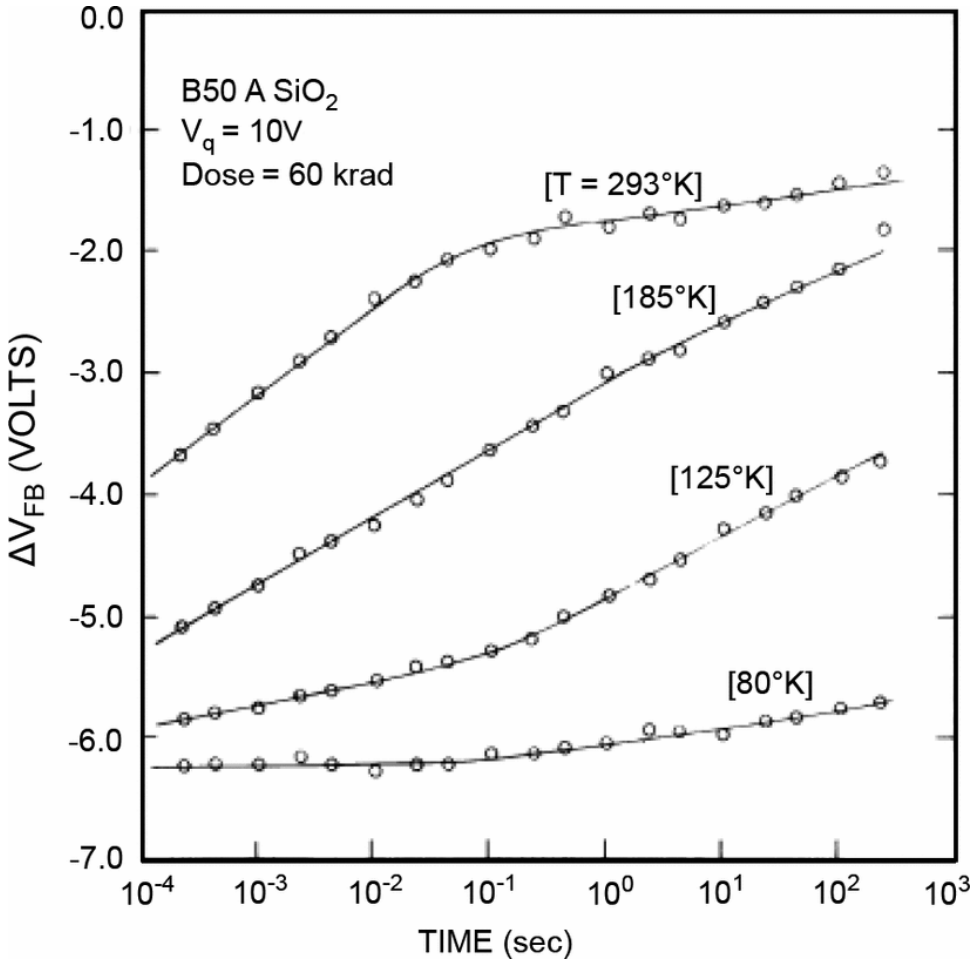
Galactic Cosmic Rays

Fractional yield of holes generated in SiO_2 as a function of electric field in the material. [H. J. Barnaby, "Total-Ionizing-Dose Effects in Modern CMOS Technologies," in *IEEE Transactions on Nuclear Science*, vol. 53, no. 6, pp. 3103-3121, Dec. 2006.]

Testing Dose Rates vs. Space Dose Rates

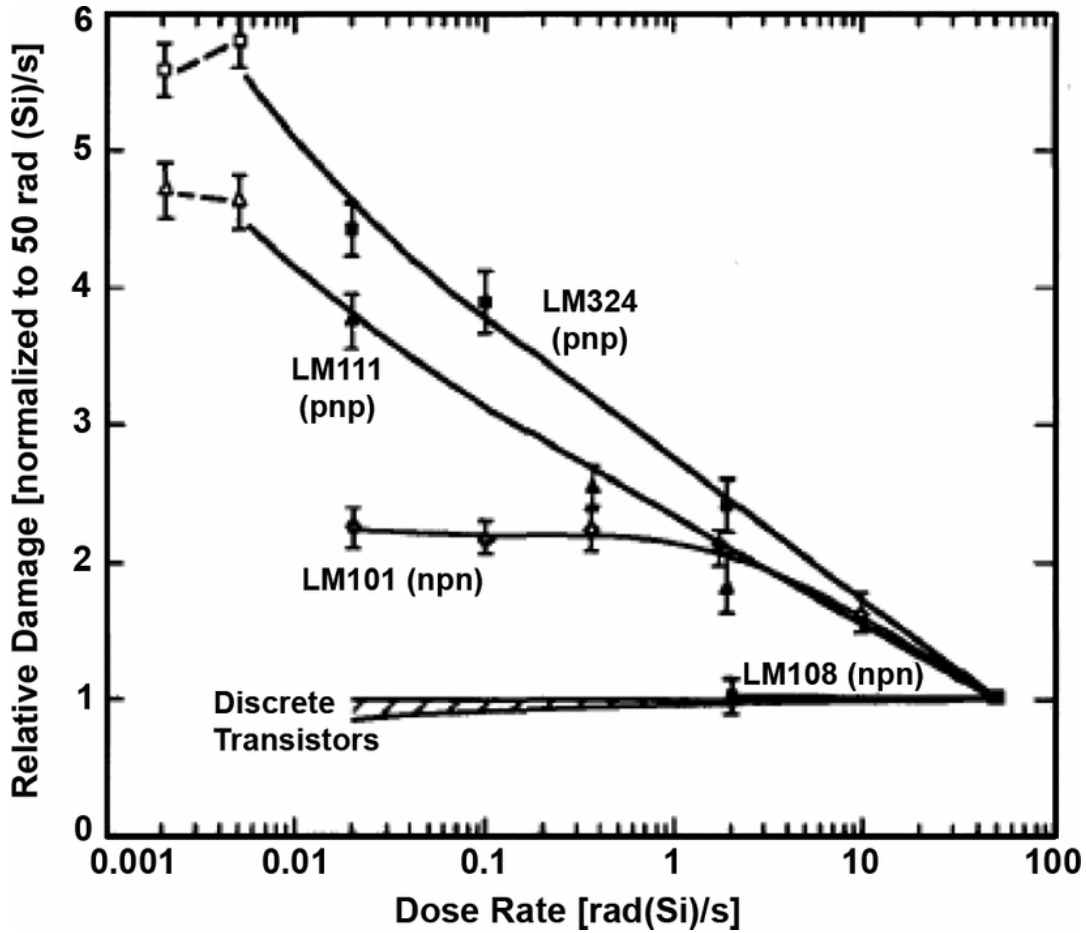
- **Dose rate is the rate in which the electronics accumulate TID**
- **In space, the dose rate is very low**
  - We cannot practically test at that dose rate
  - The dose rate for testing is >> the dose rate in space
  - This discrepancy is fine as long is there is not an issue with the dose rate
- **In 1998 it was discovered that bipolar electronics (analog, linears) are susceptible to Enhanced Low Dose Rate Sensitivity (ELDRS) [D. M. Fleetwood, "Total Ionizing Dose Effects in MOS and Low-Dose-Rate-Sensitive Linear-Bipolar Devices," in *IEEE Transactions on Nuclear Science*, vol. 60, no. 3, pp. 1706-1730, June 2013.]**
  - Several linear components had on-orbit failures after being thoroughly tested in a Co60 source
  - It was later determined that the components were more sensitivity to TID when the dose rate was at a space dose rate level than the test dose rate level

Time Effects in TID



Delta Vth as a function of radiation temperature and time. [D. M. Fleetwood, "Total Ionizing Dose Effects in MOS and Low-Dose-Rate-Sensitive Linear-Bipolar Devices," in *IEEE Transactions on Nuclear Science*, vol. 60, no. 3, pp. 1706-1730, June 2013.]

Measured ELDRS Effects in Linears



Normalized degradation, relative to responses at 50rad (SiO2), as a function of dose rate for a variety of linear bipolar transistors and integrated circuits. [D. M. Fleetwood, "Total Ionizing Dose Effects in MOS and Low-Dose-Rate-Sensitive Linear-Bipolar Devices," in *IEEE Transactions on Nuclear Science*, vol. 60, no. 3, pp. 1706-1730, June 2013.]

Examples of TID in Current Components

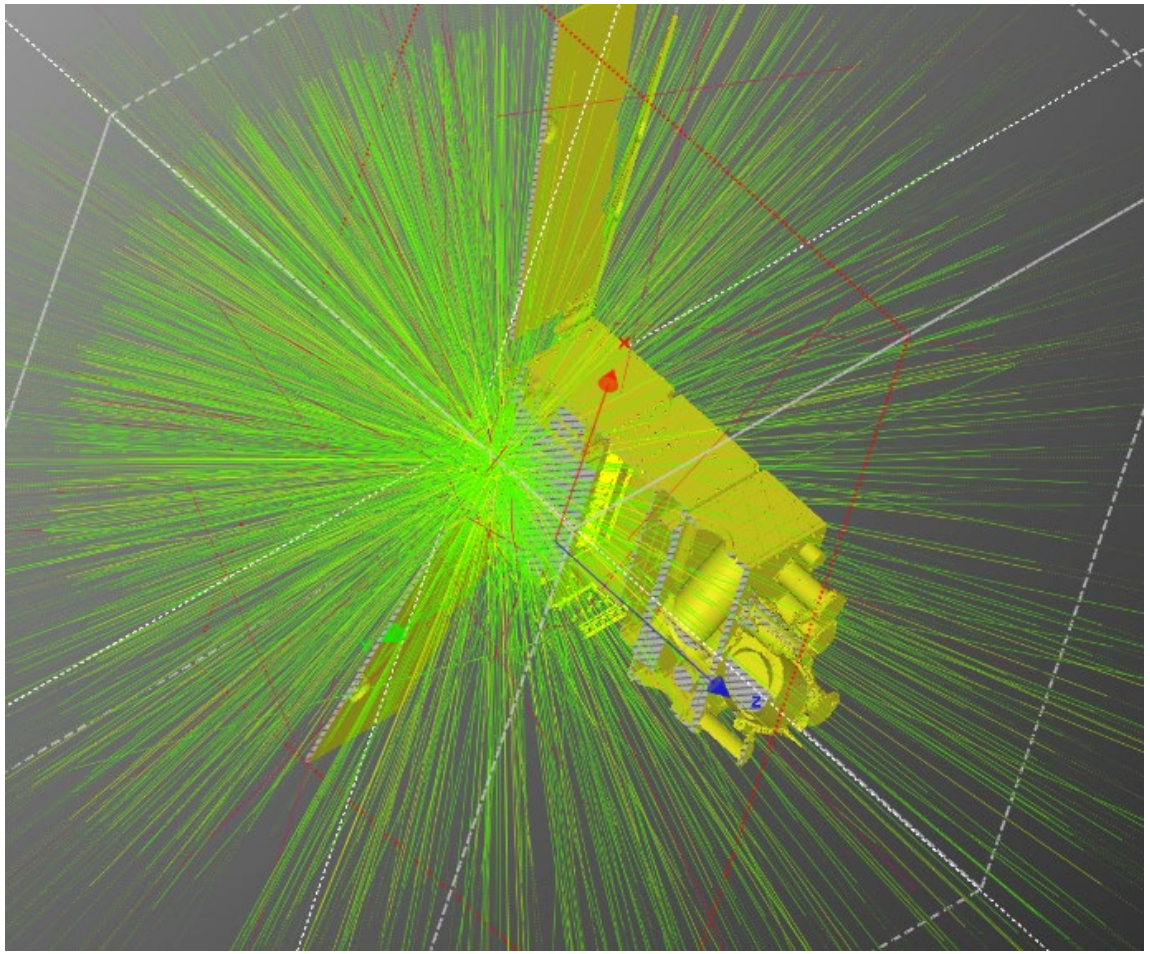
- **Analog devices:**
  - Commercial components can be as low as 5 krad(Si)
  - RHBP components can be higher
- **Memory devices**
  - Traditionally problems with non-volatile memory have been the focus
  - Flash memory handle about 20-30 krad(Si)
  - RHBP memory components that can handle 1 Mrad(Si)
- **Commercial digital processing elements (field-programmable gate arrays, microprocessors, complex CMOS):**
  - Are often 100-300 krad(Si) components, but often need testing

TID in Components

- **All electronics have a sensitivity to TID: it is a matter of threshold and testing**
- **Rad-hard or “space-grade” parts have likely been tested for TID tolerances**
  - Rad-hard does not mean ITAR, so check the data sheet to guarantee what it can tolerate
- **Many commercial parts have a reasonable TID tolerances, but the parts have to be tested to determine the sensitivity**
  - We have seen many commercial parts with very high tolerances to TID
  - We are seeing in the literature that the new finFET transistors might be more sensitive to TID than the older bulk transistors

Approach to TID in Satellites

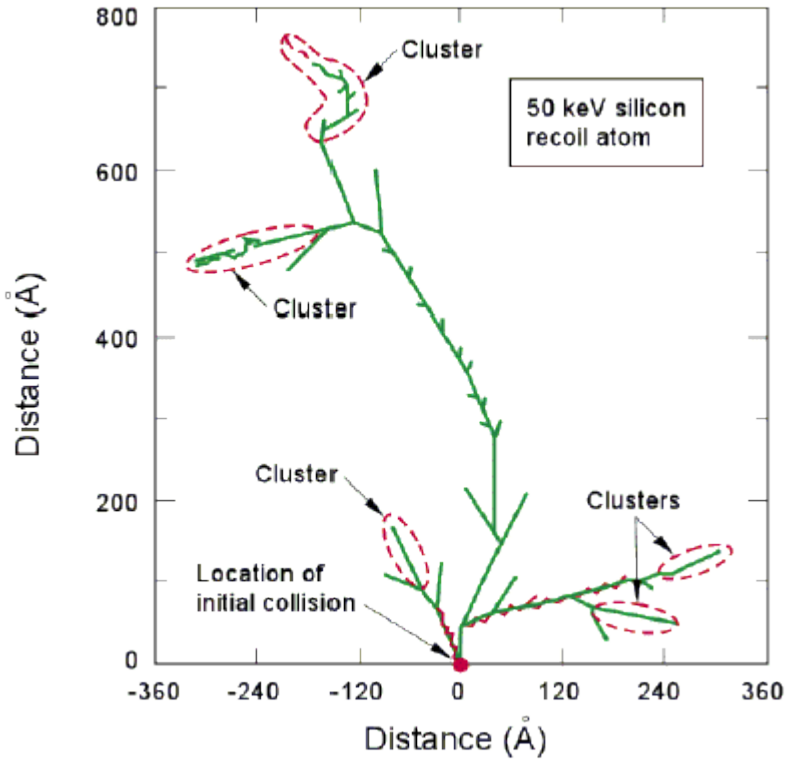
- **First step, we need to model what the interior radiation environment inside the payload to determine what the absorbed dose should be is in different areas of the payload**
  - Large effort by R&R team to validate several tools (FastRAD, NOVICE, GEANT4, MCNP)
- **Once we know the interior radiation environment, we check to make certain the components can tolerate enough ionizing dose to survive the entire mission**
  - TID is a step function (functional, non-functional)
  - Spot shielding can be useful within reason



Displacement Damage (DD) or Total Non-ionizing Dose (TNID)

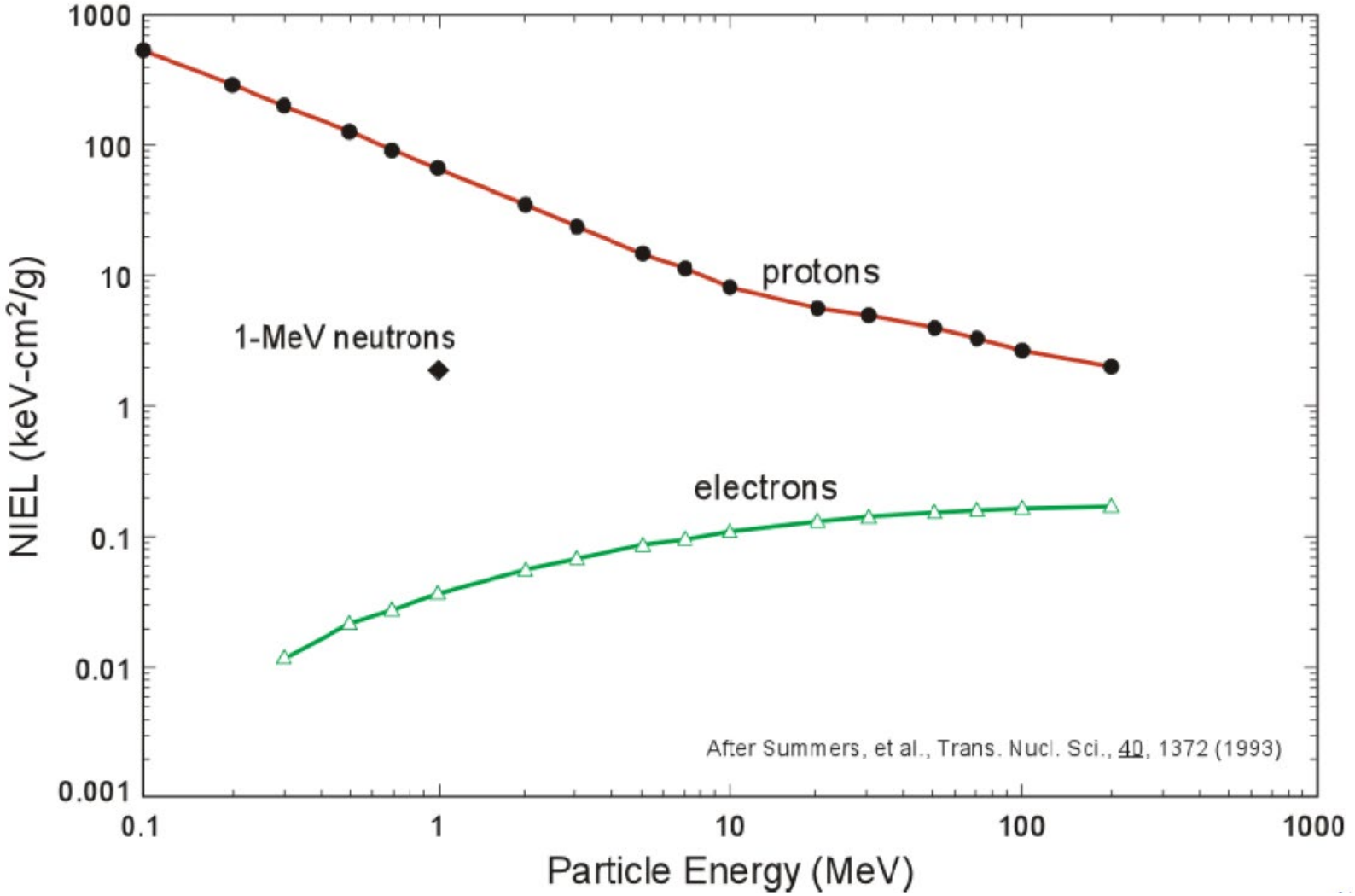
DD Mechanism

- **Heavier particles interacting with the electronics can cause damage to the rigid Silicon lattice**
- **Classical physics types of interactions:**
  - A heavy particle knocks-on a Silicon atom or a dopant and removes it from the lattice
  - In some cases, the interaction can cause a cascade of displacements
  - Over time the lattice structure is gradually turned into an amorphous crystalline structure
- **The energy involved in this interaction is the nuclear energy loss**
  - Low energy interactions most common – particle is at the end of its range and has lost most of its energy from electrical energy loss



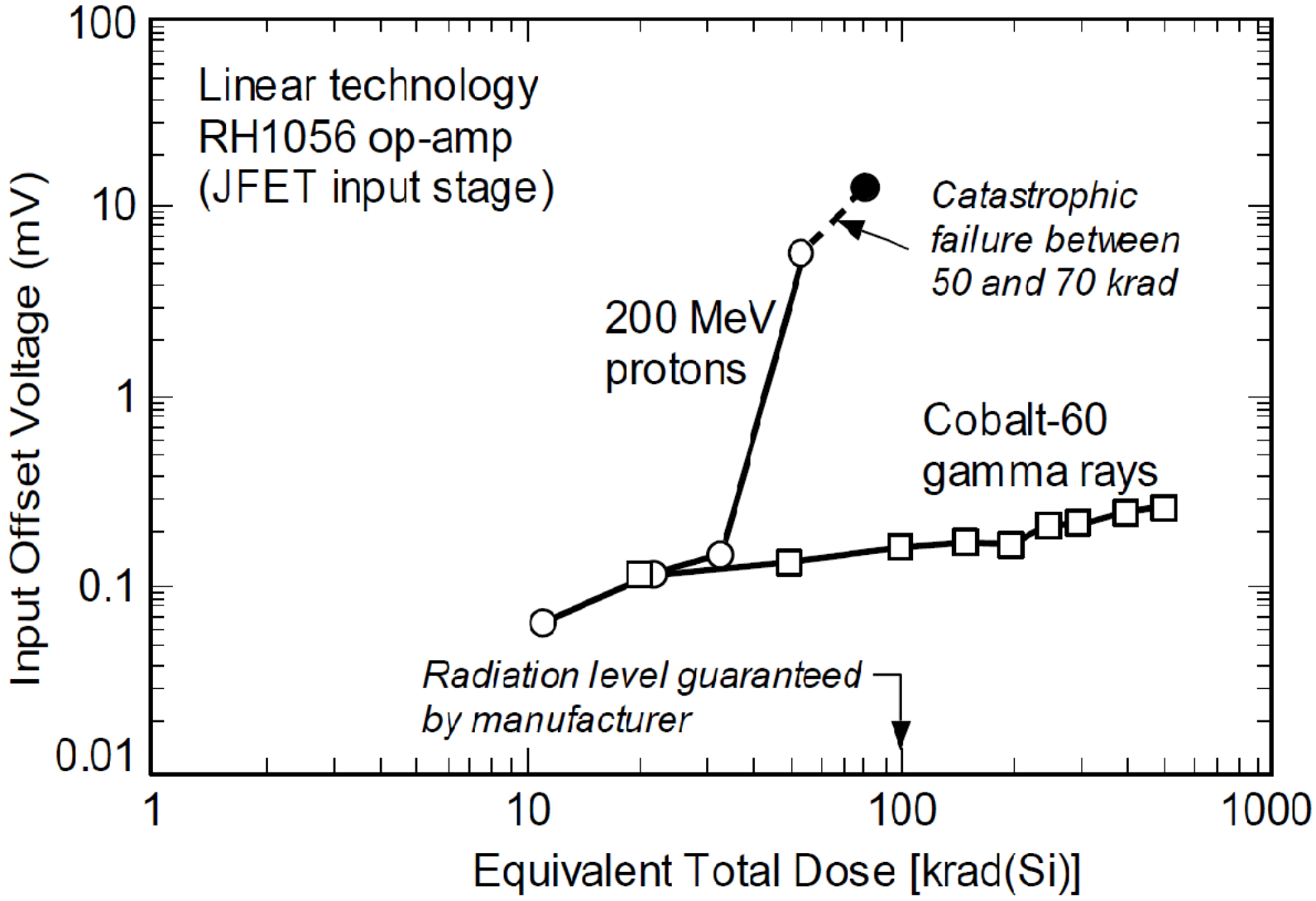
Displacement Cascade Damage in Silicon ["Space Radiation Effects on Microelectronics," NASA Jet Propulsion Laboratory]

Energy Dependence for DD



[https://parts.jpl.nasa.gov/docs/Radcrs_Final.pdf]

DD vs. TID



[https://parts.jpl.nasa.gov/docs/Radcrs_Final.pdf]

DD in Components

- **Generally takes more than 3E10 particles/cm^2 to cause a noticeable change to the components**
  - Low-earth orbit in the trapped proton belt
  - Prompt dose effect from manmade nuclear environments
- **Analog components appear to have more problems than CMOS components**
- **We've had DD problems at LANSCE after a few days of testing**
  - The parts are not completely non-functional, but are no longer stable

Approach to DD in Satellites

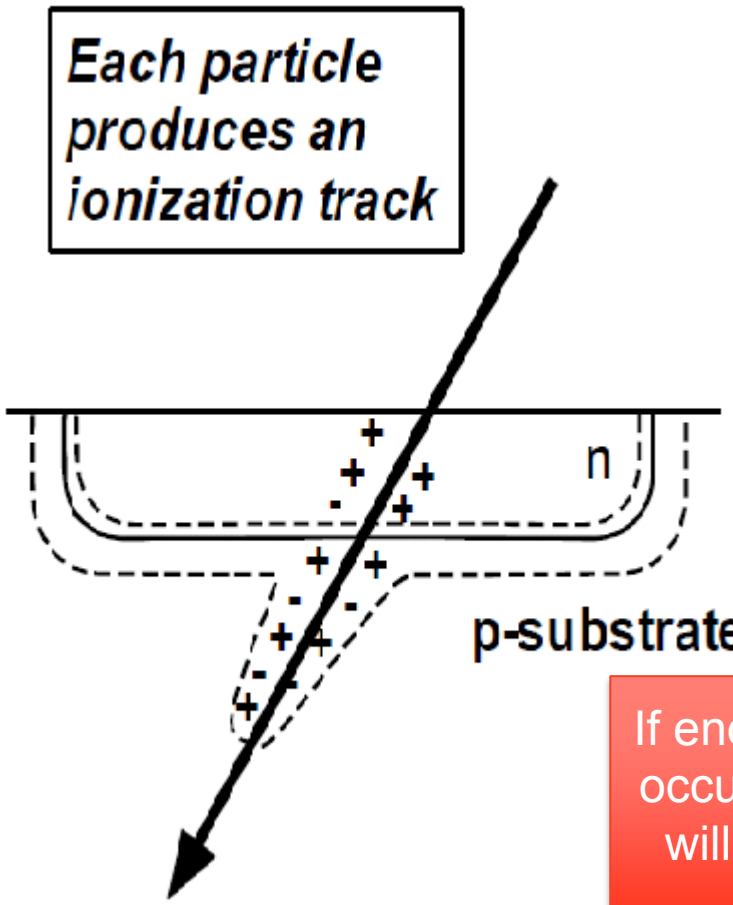
- **There is no first step: most of this radiation cannot be shielded**
- **We check to make certain the components can tolerate enough 1-MeV neutron equivalents as specified in the requirements**
  - DD tends to be a step function (functional, non-functional)

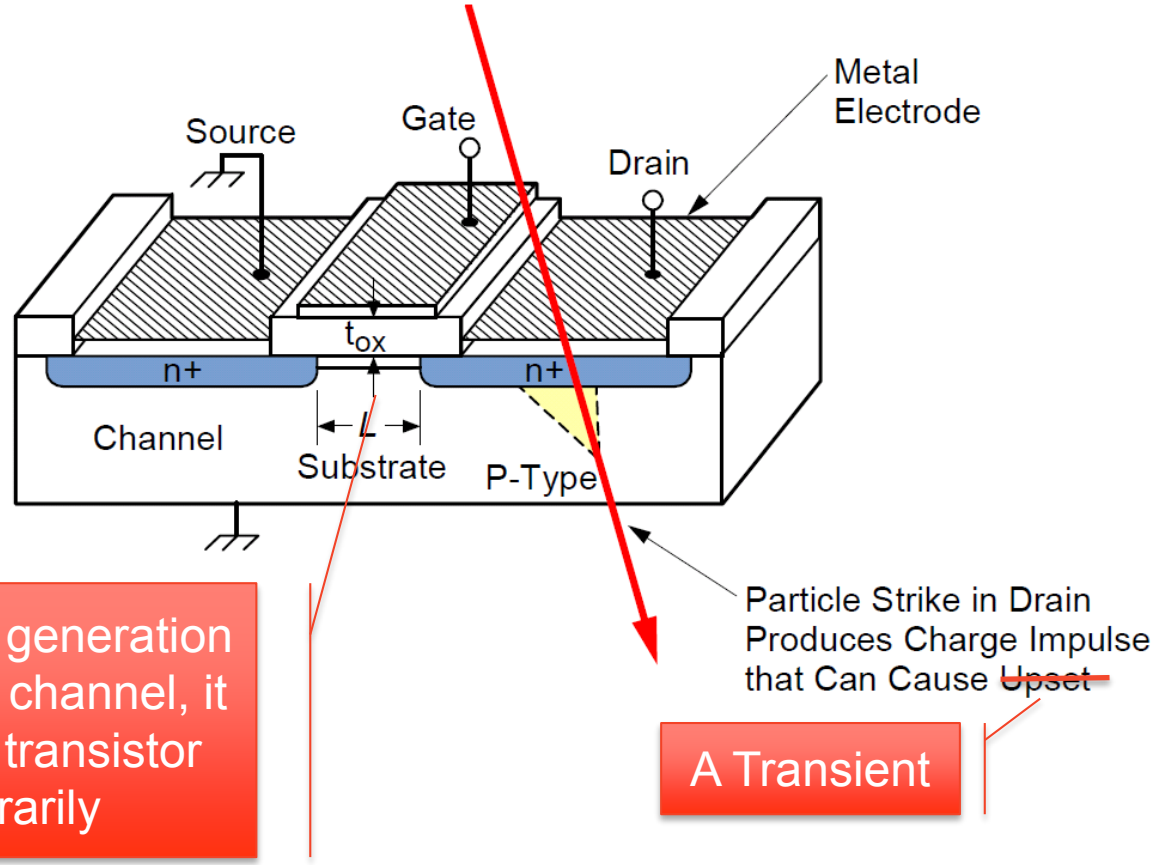
Single-Event Effects (SEEs)

Single-Event Effects (SEEs)

- **Currently, neck and neck with TID for top problem for satellites**
  - Caused by many forms of charged particles and neutrals
- **SEEs is an umbrella term that covers about 10 different types of effects**
- **The root mechanism comes from EHPS causing charge generation in the transistor**
  - Transistor on: a little overcurrent, but no problem
  - Transistor off: transistor turns on

SEE Mechanism

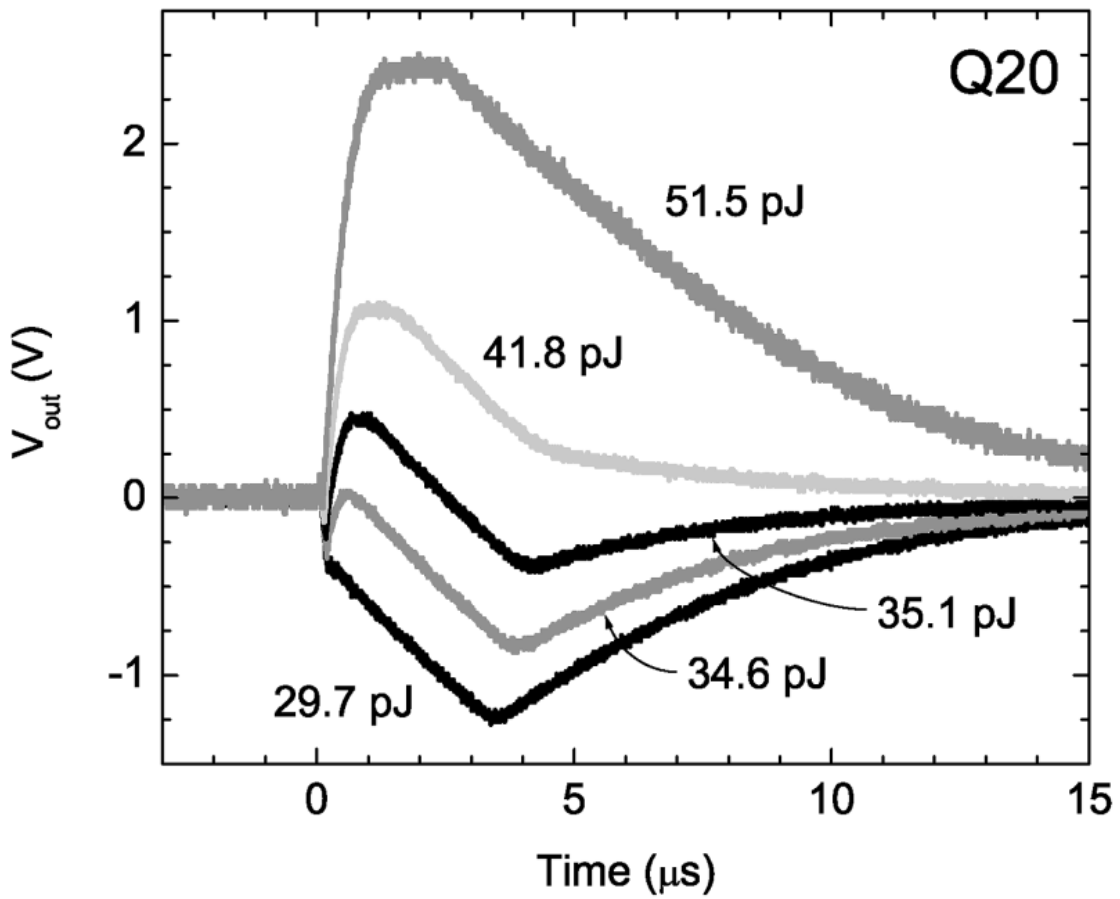




If enough charge generation occurs under the channel, it will turn an “off” transistor “on” temporarily

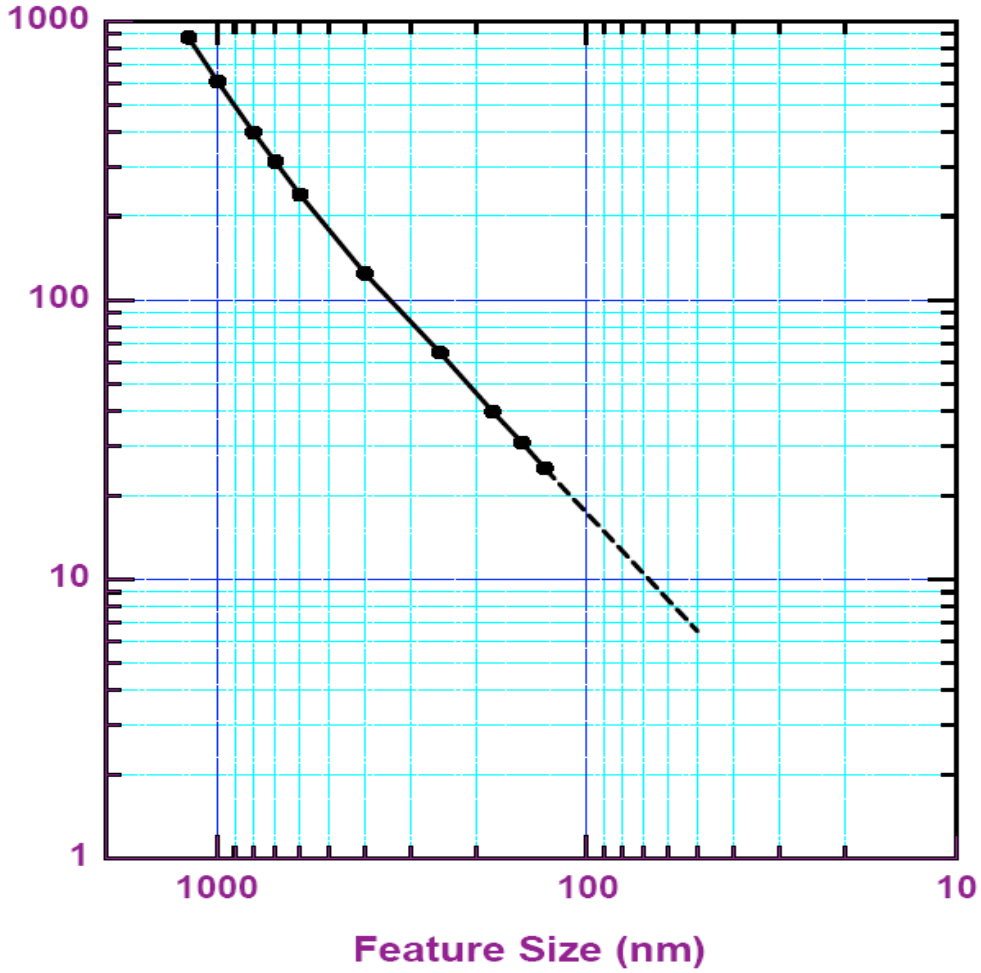
[https://parts.jpl.nasa.gov/docs/Radcrs_Final.pdf]

How Temporarily?



Q20 SET waveform for different laser energies for 815-nm laser, [R. L. Pease *et al*., "Comparison of SETs in bipolar linear circuits generated with an ion microbeam, laser light, and circuit simulation," in *IEEE Transactions on Nuclear Science*, vol. 49, no. 6, pp. 3163-3170, Dec 2002.]

Critical Pulse Width for Unattenuated Propagation



Mavis, "Single-Event Transient Phenomena: Challenges and Solutions." MRQW, 2002.

Does This Transient Matter?

- **Depends on the circuit and the transient location**
  - More logic: the transient might dampen or might not
  - A latch: the transient might “latch” and become state
  - The transient is inside of a memory cell: the transient only needs to last long enough to change the inverter value to lead to persistent memory value change
  - The transient is in one of the extra transistors we were talking about: the transient might cause permanent damage to the component
- **What we are talking about is a single-event transient (SET) and it is the ur mechanism for all single-event effects (SEE)**
  - SET in memory causes single-event upsets (SEUs), which are memory bitflips
  - SET in the extra vertical transistor under the source or drain causes single-event latchup (SEL)
  - SET in the extra transistor in the mesa structure of a power MOSFET causes single-event burnout (SEB) or single-event gate rupture (SEGR)

SEUs

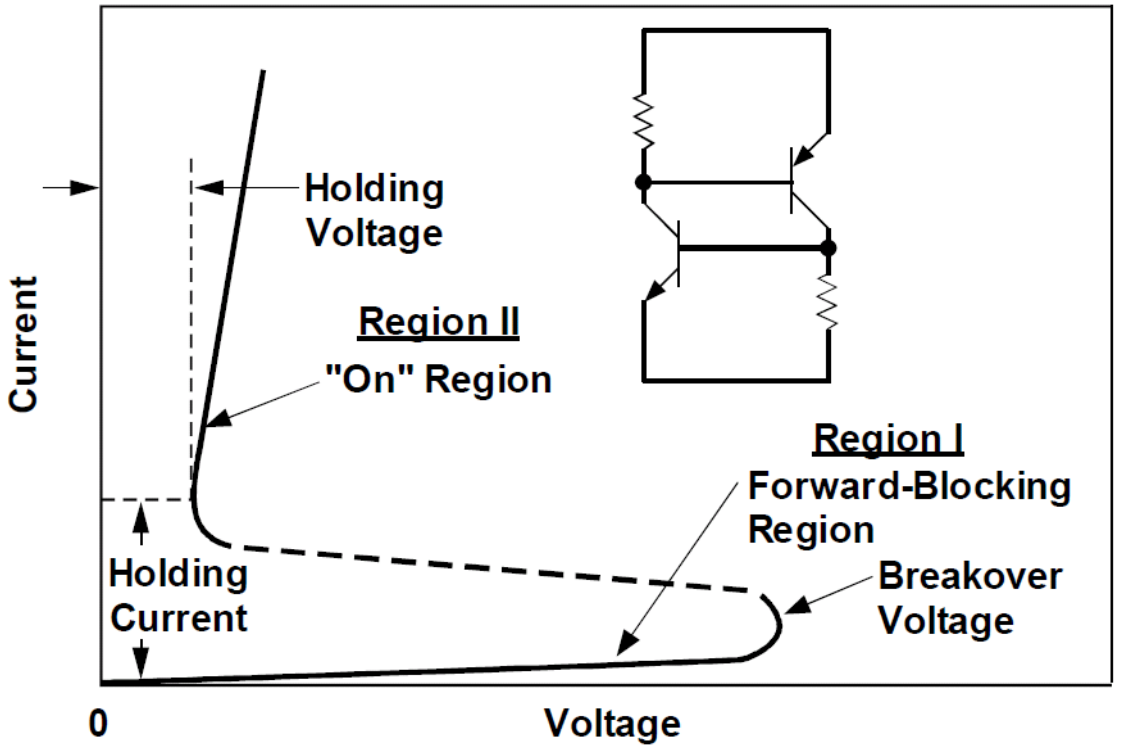
- **As described on the previous slide, an SEU is essentially an SET that is immediately latched**
- **Virtually all types of electronics with memory in them have SEUs**
  - SEUs are also starting to be found in digital/analog converters
  - SEUs in control logic are also common
  - SEUs in dynamic memory are common, although the mechanism is different
- **As transistors have shrunk, RHBP and radiation-hardened by design (RHBD) methodologies have been unable to suppress SEU response in electronics**
- **In recent components, many SEUs are multiple-cell upsets, where multiple SRAM bits change values**
  - The charge generation is moving through the substrate and affecting multiple bits

SEFIs

- **Often caused by SEUs or SETs in control circuitry of a device**
- **While SEFIs are unique to the component, nearly all types of processing components have these types of SEFIs:**
  - Power-on-reset: SEU/SET to circuitry that allows for a soft or hard reset of the component
  - JTAG: Circuit that is common for all electronics for debugging the hardware
- **Dynamic memory has a particular vicious SEFI state that can corrupt 1,000s of words such that error correction is not possible**
- **Components are not "self-aware" and usually need external components to detect and correct SEFI states**
- **Side effects of SEFIs:**
  - Component functions improperly, including resetting, shutting down, resetting all memory values to zero, outputting garbage values
  - When is an SEU a SEFI?

SEL

- **To some degree latchup is just part of CMOS**
  - Old times: used to latch parts on the bench electrically
  - Middle years: Designers “tapped” the wells which effectively put a resistor across the vertical transistor to reduce electrical latchup
  - Modern years: tapping takes too much space, and all sorts of latchup is common again
- **SEL can be catastrophic for components**
  - Only way to recover is to power cycle the component
  - In testing, we put the components on a programmable power supply with a millisecond trigger to power cycle on the event of a current pulse and we destroy parts



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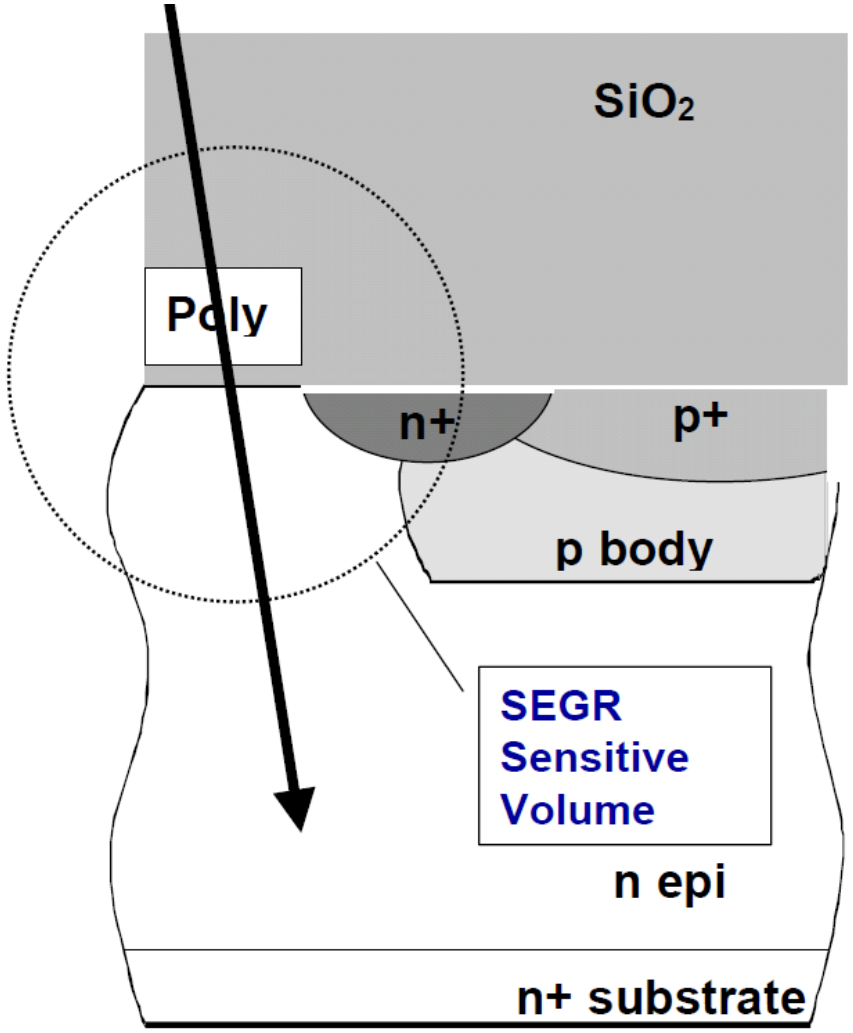
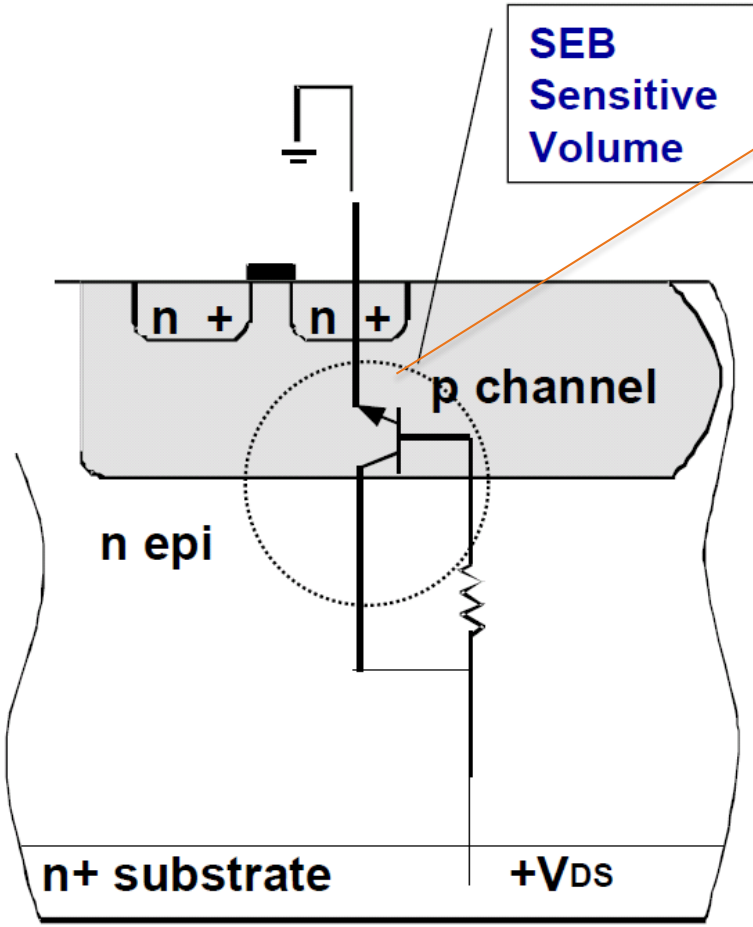
SEB/SEGR



Single Event Gate Rupture Power MOSFET



Single Event Burnout HEXFET

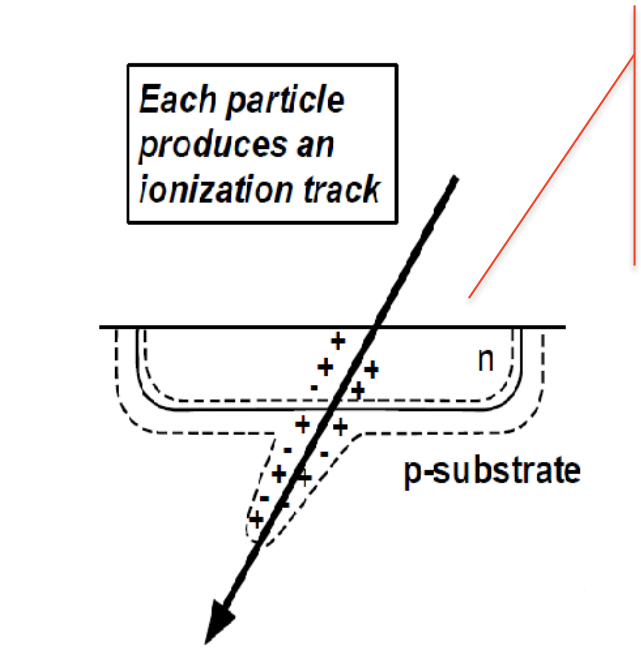
[https://parts.jpl.nasa.gov/docs/Radcrs_Final.pdf]

In both cases, testing is difficult because the extra transistors are buried. Space radiation has no problem reaching those transistors

More likely to be destructive in high-voltage power MOSFETS (due to inability derate), but we do have problems with the charge pumps in flash

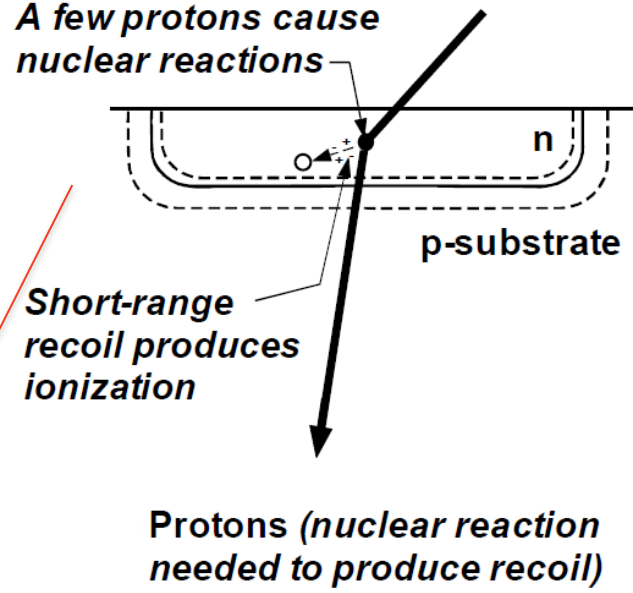
Types of Radiation and SEE Efficiency

- To a certain degree, it is part specific
- In the original image showing charge generation, the EHPS are being generated through direct ionization: the charged particle is causing the EHP production
- In the new image, the EHPS are being generated through indirection ionization: the neutron or proton cause a nuclear recoil with the Si atoms and it is the recoil atom that causes the EHP production
- As transistors have decreased in size, the onset threshold to SEE has decreased
- For awhile the sensitivities were also increasing, but manufacturers started seeing more problems with neutrons so altered their designs to be naturally less sensitive to neutrons



Heavy ions: > 0.1 LET
Protons: ~0.1 MeV
Muons: ? MeV
Electrons: > 20 MeV

Most protons pass through the device with little effect



Neutrons: > 0.1 MeV
Protons: >3 MeV

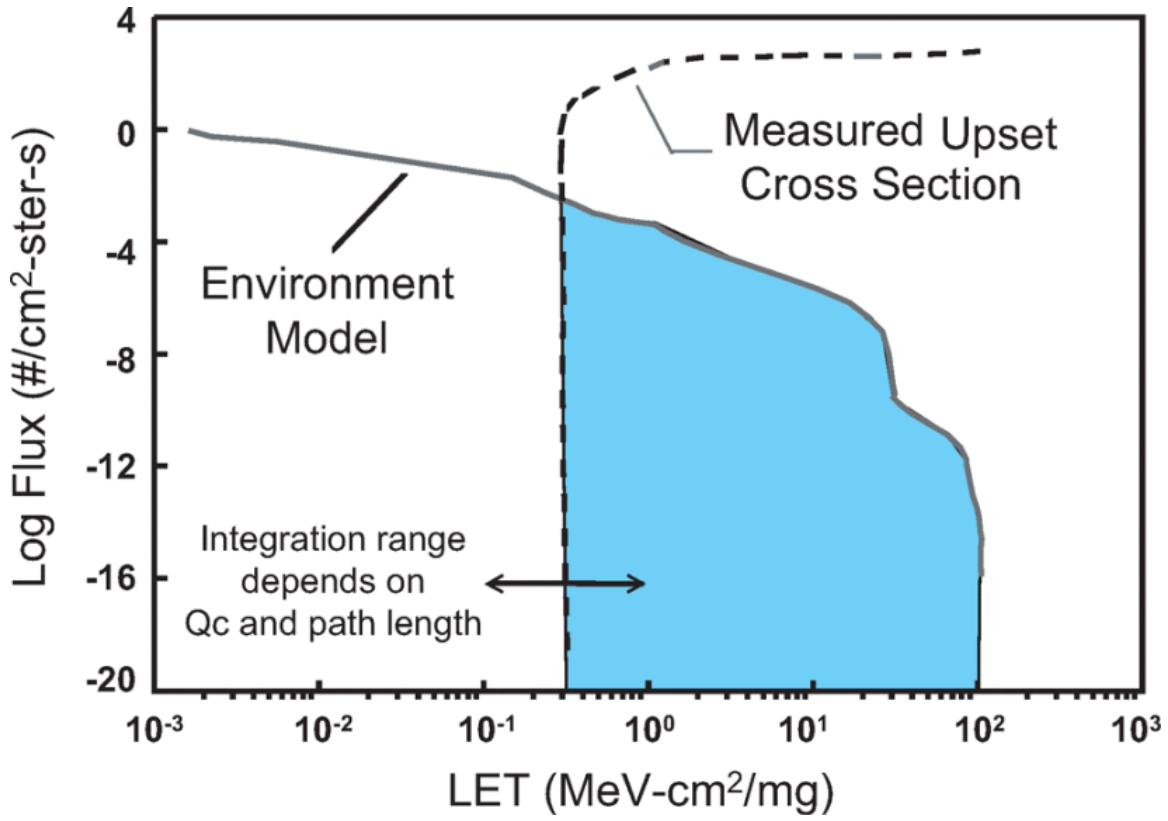
Protons *(nuclear reaction needed to produce recoil)*

SEE in Components

- **Most digital and analog components have some form of SEE**
  - Traditionally we fly rad-hard parts to avoid these issues, but even rad-hard parts have SEUs, SETs, and SEFIs these days
  - Many of the parts we fly are upscreened commercial parts, and will have at least SEUs, SETs, SEFIs
- **Some families of parts have issues with particular SEE types**
  - High-voltage power MOSFETS and diodes have SEB and SEGR sensitivities
  - Analog components tend to be sensitive to SEL and SETs
  - Memory components have SEUs and SEFIs
  - DRAM components have SEU, SEDD and SEFIs
  - Processing elements have SEL, SEU, SETs, and SEFIs
- **As we can no longer easily avoid these issues, we need to build our systems to be more resilient to SEE faults and/or quickly recover from SEE faults**

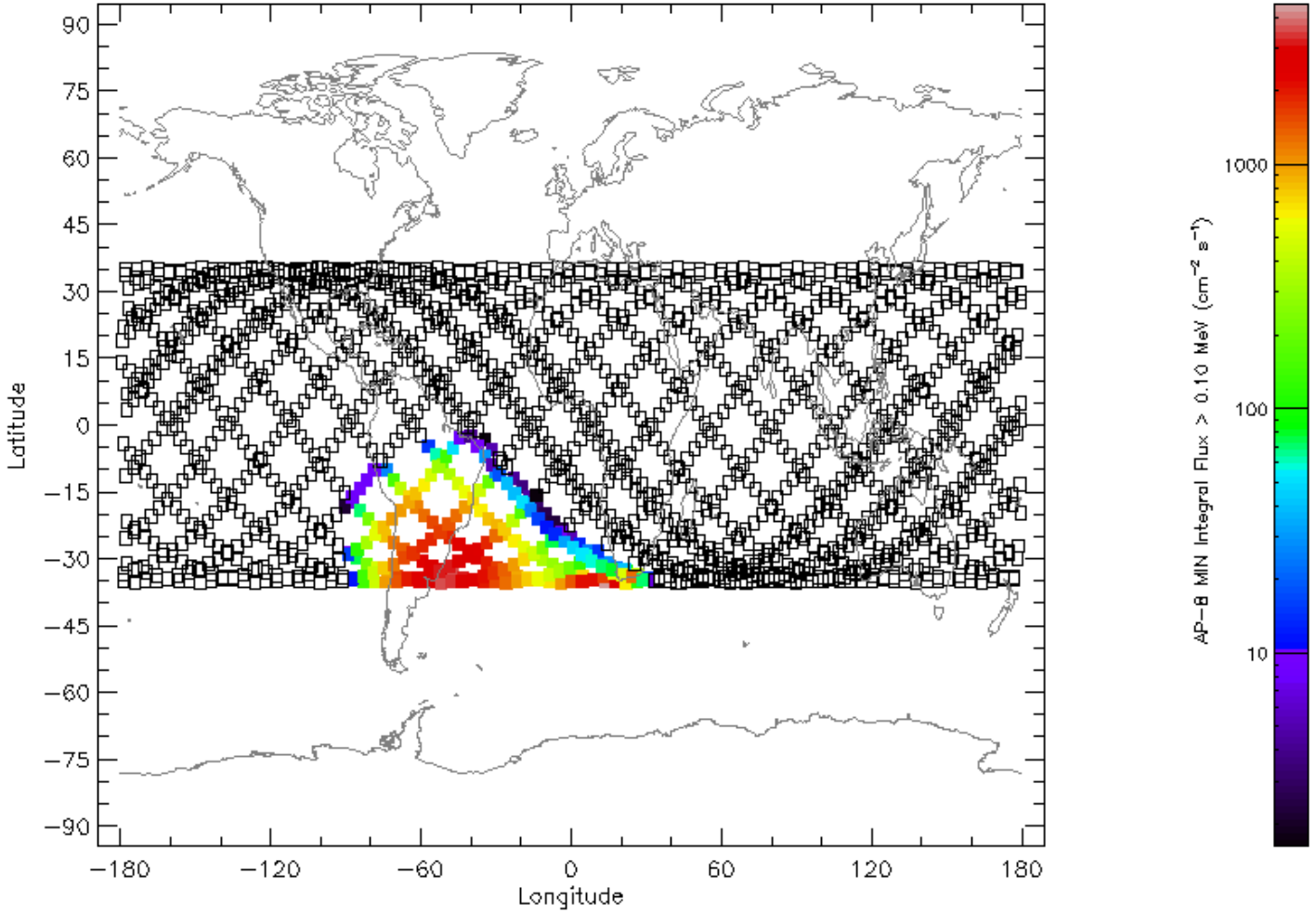
Approach to SEE in Satellites

- **The first step, is to model the radiation environment**
  - Shielding will not help SEE, but knowing the radiation environment will help us determine the expected on-orbit failure rate
- **We use information about the parts and environment to determine the average mean-time to event**
- **SEE faults are stochastic by nature: we cannot predict when it will occur**
  - The occurrences will average out over time, but it can take a long time to average out
  - For less common events, it may never average out during the mission

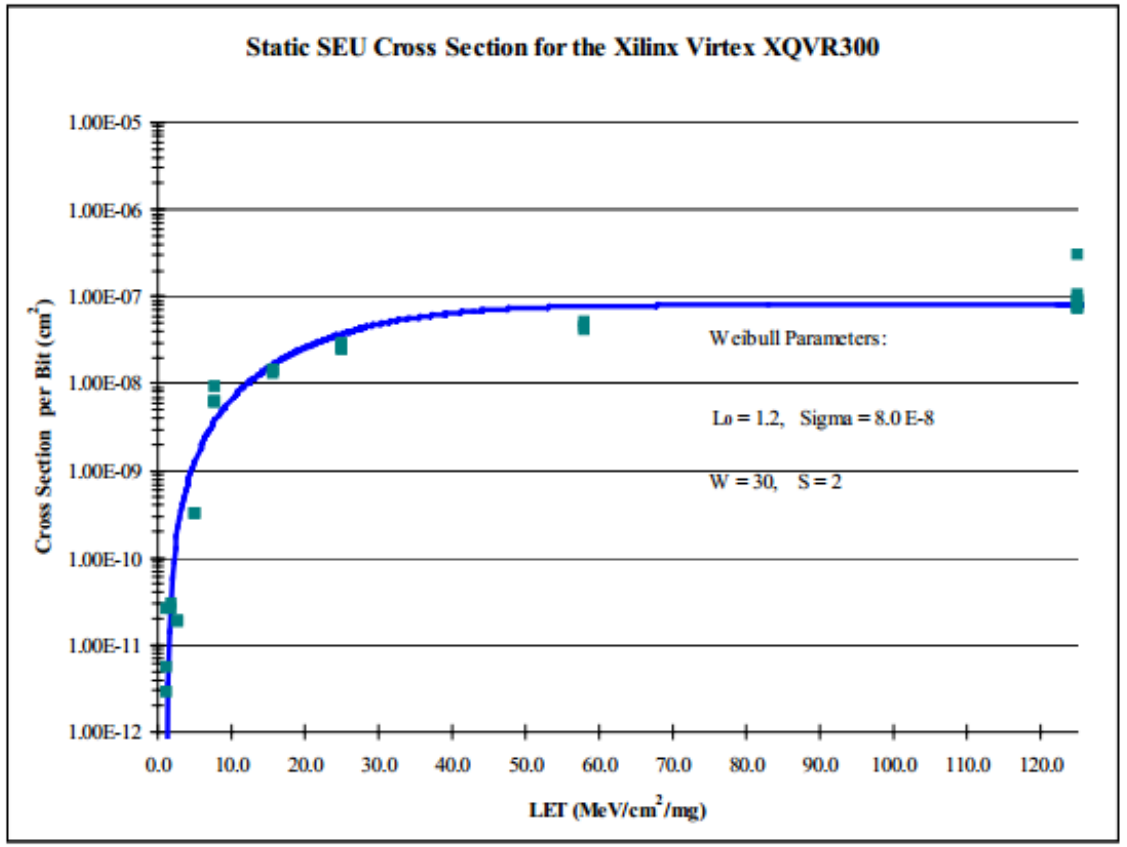


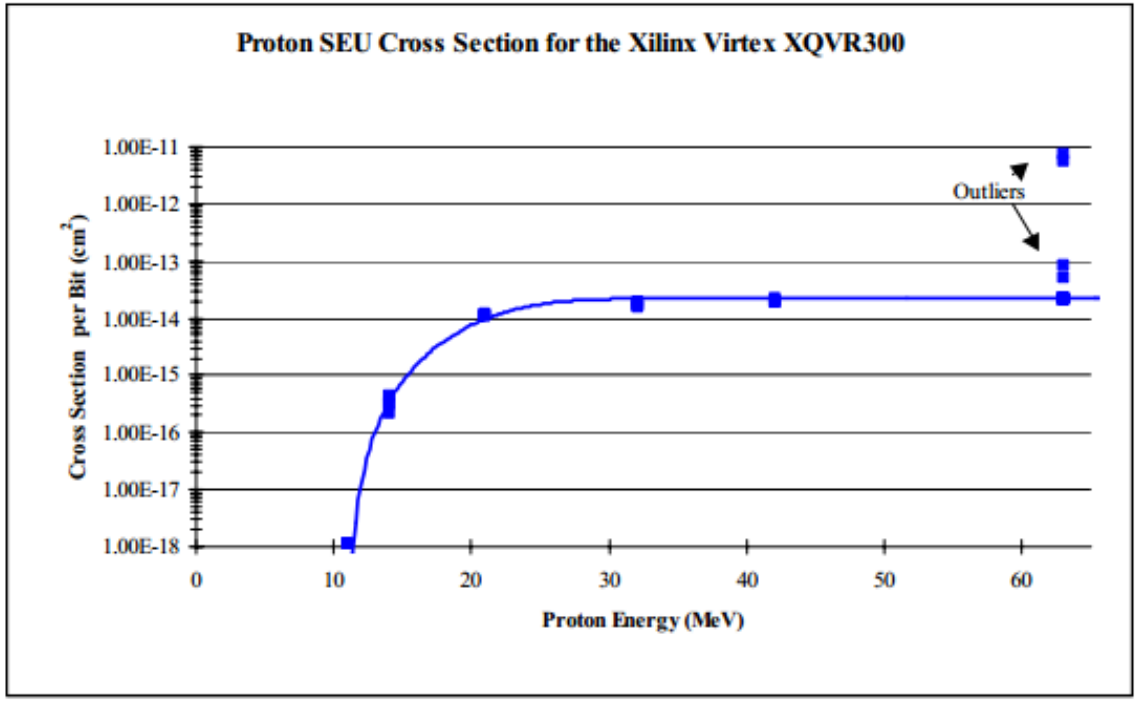
Measured upset error cross section and particle flux for a hypothetical space environment. The error rate is determined by convolving the environment model with the error cross section. [J. R. Schwank, M. R. Shaneyfelt and P. E. Dodd, "Radiation Hardness Assurance Testing of Microelectronic Devices and Integrated Circuits: Radiation Environments, Physical Mechanisms, and Foundations for Hardness Assurance," in IEEE Transactions on Nuclear Science, vol. 60, no. 3, pp. 2074-2100, June 2013.]

Cibola Flight Experiment (CFE) Environment



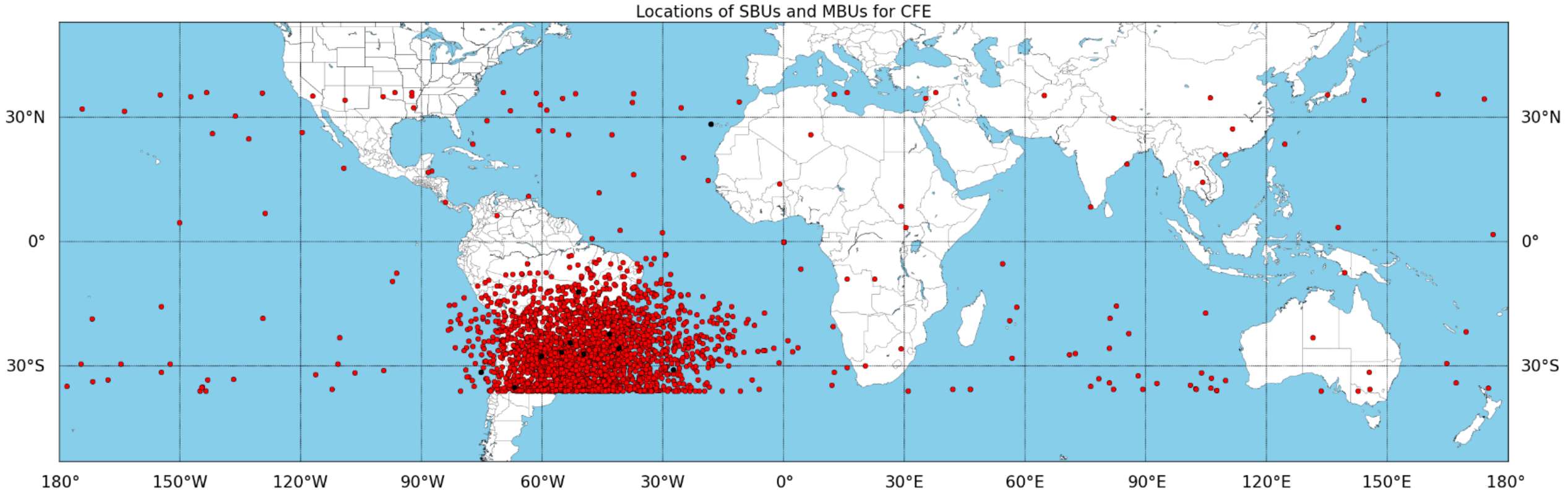
SEU Cross Sections for Virtex FPGAs



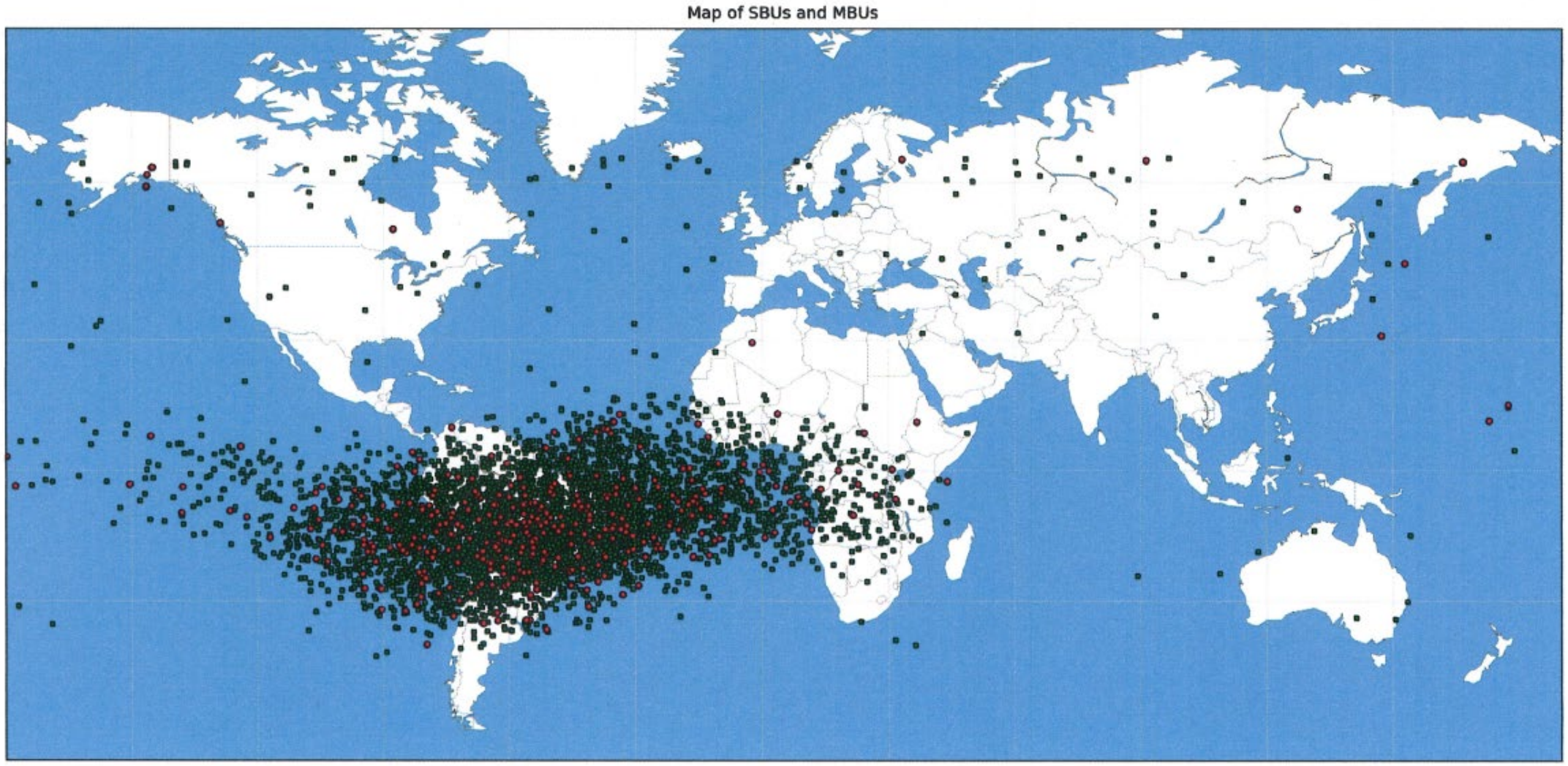


How bad were the SEUs from this component?

Locations of SEUs in FPGAs on CFE: 3/2007-6/2014



Technology Is Not on Our Side:
SEUs on the Mission Response Module in the First Year



Conclusions

- **Radiation effects for satellites continue to be a challenge, but extensive testing and modeling allows satellite designers to build robust systems that can survive the space weather environment**
  - TID: permanent degradation from charged particles
  - DD: permanent degradation from heavier particles
  - SEE: permanent or temporary failures from heavy ions, protons, neutrons, muons, and electrons